AMENDMENTS TO THE CLAIMS

1. (Previously Presented) An ESD protection device comprising:

a substrate;

an isolation region on the substrate, enclosing an active region;

a first gate having two ends overlapping the isolation region to stretch over the active region, and coupled to a first node;

a second gate disposed on a first side of the first gate and near the first end of the first gate; and

first and second doping regions at the first and second sides of the first gate, and coupled to a second and the first node respectively, wherein the first doping region has a first discontinuity region, without source/drain implantation, in the substrate under the second gate.

2. (Original) The ESD protection device as claimed in claim 1, wherein the isolation region is a shallow trench isolation.

3. (Original) The ESD protection device as claimed in claim 1, wherein the first node is ground while the second node is a pad.

4. (Previously Presented) The ESD protection device as claimed in claim 1 further comprising:

a third gate disposed at the first side of the first gate and near the second end of the first gate, wherein the first doping region has a second discontinuity region, without source/drain implantation, in the substrate under the third gate.

5. (Previously Presented) The ESD protection device as claimed in claim 4 further comprising:

a fourth gate having a first and second end overlapping the isolation region to stretch over the active region, and coupled to the first node, wherein the first doping region is between the first and fourth gate;

a fifth and sixth gate both disposed at a first side of the fourth gate, and respectively near a first and second end of the fourth gate, wherein the first doping region has a third and fourth discontinuity region, without source/drain implantation, respectively in the substrate under the fifth and sixth gate; and

a third doping region on a second side of the fourth gate and coupled to the second node.

6. (Original) The ESD protection device as claimed in claim 5, wherein each of the second, third, fifth and sixth gate has one end overlapping the isolation region.

7. (Original) The ESD protection device as claimed in claim 5, wherein each of the first, second, third, fourth, fifth and sixth gate comprises:

a conducting layer;

a gate oxide layer under the conducting layer; and

a first and second spacer respectively adjacent to two sides of the conducting layer and gate oxide layer.

8. (Original) The ESD protection device as claimed in claim 7, wherein the conducting layer is a polysilicon layer while the gate oxide layer, and the first and second spacer are silicon oxide layers.

9. (Original) The ESD protection device as claimed in claim 1 further comprising a fourth doping region enclosing the isolation region.

10. (Original) The ESD protection device as claimed in claim 9, wherein the substrate is a P substrate, the first, second and third doping region are N doping regions, and the fourth doping region is a P doping region.

11. (Previously Presented) An ESD protection device comprising:

a substrate;

an isolation region on the substrate, enclosing an active region;

a first gate having two ends overlapping the isolation region to stretch over the active region, and coupled to a first node;

a second gate disposed on a second side of the first gate and near the first end of the first gate; and

first and second doping regions at the first and second sides of the first gate, and coupled to a second and the first node respectively, wherein the second doping region has a first discontinuity region, without source/drain implantation, in the substrate under the second gate.

12. (Original) The ESD protection device as claimed in claim 11, wherein the isolation region is a shallow trench isolation.

13. (Original) The ESD protection device as claimed in claim 11, wherein the first node is ground while the second node is a pad.

14. (Previously Presented) The ESD protection device as claimed in claim 11 further comprising:

a third gate disposed at the second side of the first gate and near the second end of the first gate, wherein the second doping region has a second discontinuity region, without source/drain implantation, in the substrate under the third gate.

15. (Currently Amended) The ESD protection device as claimed in claim 14 further comprising:

a fourth gate having a first and second end overlapping the isolation region to stretch over the active region, and coupled to the first node, wherein the first doping region is between the first and fourth gate;

a fifth and sixth gate both disposed at a first side of the fourth gate, and respectively near a first and second end of the fourth gate; and

a third doping region on the first side of the fourth gate, coupled to the second node, and having a third and fourth discontinuity region, without source/drain ~~implatation~~implantation, respectively in the substrate under the fifth and sixth gate.

16. (Original) The ESD protection device as claimed in claim 15, wherein each of the second, third, fifth and sixth gate has one end overlapping the isolation region.

17. (Original) The ESD protection device as claimed in claim 15, wherein each of the first, second, third, fourth, fifth and sixth gate comprises:

a conducting layer;

a gate oxide layer under the conducting layer; and

a first and second spacer respectively adjacent to two sides of the conducting layer and gate oxide layer.

18. (Original) The ESD protection device as claimed in claim 17, wherein the conducting layer is a polysilicon layer while the gate oxide layer, and the first and second spacer are silicon oxide layers.

19. (Original) The ESD protection device as claimed in claim 11 further comprising a fourth doping region enclosing the isolation region.

20. (Original) The ESD protection device as claimed in claim 19, wherein the substrate is a P substrate, the first, second and third doping region are N doping regions, and the fourth doping region is a P doping region.

21. (Previously Presented) An ESD protection device comprising:

a substrate;

an isolation region on the substrate, enclosing an active region;

a first gate having two ends overlapping the isolation region to stretch over the active region, and coupled to a first node; and

first and second doping regions at the first and second sides of the first gate, and coupled to a second and the first node respectively, wherein the first doping region has a first discontinuity region near the first end of the first gate.

22. (Original) The ESD protection device as claimed in claim 21, wherein the isolation region is a shallow trench isolation.

23. (Original) The ESD protection device as claimed in claim 21, wherein the first node is ground while the second node is a pad.

24. (Previously Presented) The ESD protection device as claimed in claim 21, wherein the first doping region further has a second discontinuity region near the second end of the first gate.

25. (Previously Presented) The ESD protection device as claimed in claim 24 further comprising:

a second gate having a first and second end overlapping the isolation region to stretch over the active region, and coupled to the first node, wherein the first doping region is on a first side of the second gate; and

a third doping region on a second side of the second gate, coupled to the second node;

wherein the first doping region has a third and fourth discontinuity region respectively near the first and second end of the second gate.

26. (Previously Presented) The ESD protection device as claimed in claim 25, wherein each of the first, second, third and fourth discontinuity region has one end connected to the isolation region.

27. (Original) The ESD protection device as claimed in claim 26, wherein each of the first and second gate comprises:

a conducting layer;

a gate oxide layer under the conducting layer; and

a first and second spacer respectively adjacent to two sides of the conducting layer and gate oxide layer.

28. (Original) The ESD protection device as claimed in claim 27, wherein the conducting layer is a polysilicon layer while the gate oxide layer, and the first and second spacer are silicon oxide layers.

29. (Original) The ESD protection device as claimed in claim 21 further comprising a fourth doping region enclosing the isolation region.

30. (Original) The ESD protection device as claimed in claim 29, wherein the substrate is a P substrate, the first, second and third doping region are N doping regions, and the fourth doping region is a P doping region.

31. (Previously Presented) An ESD protection device comprising:

a substrate;

an isolation region on the substrate, enclosing an active region;

a first gate having two ends overlapping the isolation region to stretch over the active region, and coupled to a first node; and

first and second doping regions at the first and second sides of the first gate, and coupled to a second and the first node respectively, wherein the second doping region has a first discontinuity region near the first end of the first gate.

32. (Original) The ESD protection device as claimed in claim 31, wherein the isolation region is a shallow trench isolation.

33. (Original) The ESD protection device as claimed in claim 31, wherein the first node is ground while the second node is a pad.

34. (Original) The ESD protection device as claimed in claim 31, wherein the second doping region further has a second discontinuity region near the second end of the first gate.

35. (Previously Presented) The ESD protection device as claimed in claim 34 further comprising:

a second gate having a first and second end overlapping the isolation region to stretch over the active region, and coupled to the first node, wherein the first doping region is at a first side of the second gate; and

a third doping region at a second side of the second gate, coupled to the second node;

wherein the second doping region has a third and fourth discontinuity region respectively near the first and second end of the second gate.

36. (Previously Presented) The ESD protection device as claimed in claim 35, wherein each of the first, second, third and fourth discontinuity regions has one end connected to the isolation region.

37. (Original) The ESD protection device as claimed in claim 36, wherein each of the first and second gates comprises:

38. (Original) The ESD protection device as claimed in claim 37, wherein the conducting layer is a polysilicon layer while the gate oxide layer, and the first and second spacer are silicon oxide layers.

39. (Original) The ESD protection device as claimed in claim 31 further comprising a fourth doping region enclosing the isolation region.

40. (Original) The ESD protection device as claimed in claim 39, wherein the substrate is a P substrate, the first, second and third doping region are N doping regions, and the fourth doping region is a P doping region.

41. (Previously Presented) An ESD protection device comprising:

a substrate;

an isolation region on the substrate, enclosing an active region;

a first gate having two ends overlapping the isolation region to stretch over the active region, and coupled to a first node; and

first and second doping regions at the first and second sides of the first gate, and coupled to a second and the first node respectively;

wherein the isolation region protruding into the first doping region near the first end of the first gate.

42. (Original) The ESD protection device as claimed in claim 41, wherein the isolation region is a shallow trench isolation.

43. (Original) The ESD protection device as claimed in claim 41, wherein the first node is ground while the second node is a pad.

44. (Original) The ESD protection device as claimed in claim 41, wherein the isolation region protruding into the first doping region near the second end of the first gate.

45. (Original) The ESD protection device as claimed in claim 44 further comprising:

a second gate having a first and second end overlapping the isolation region to stretch over the active region, and coupled to the first node, wherein the first doping region is on a first side of the second gate; and

a third doping region on a second side of the second gate, coupled to the second node;

wherein the isolation region protruding into the first doping region near the first and second end of the second gate.

46. (Original) The ESD protection device as claimed in claim 45, wherein each of the first and second gate comprises:

a conducting layer;

a gate oxide layer under the conducting layer; and

a first and second spacer respectively adjacent to two sides of the conducting layer and gate oxide layer.

47. (Original) The ESD protection device as claimed in claim 46, wherein the conducting layer is a polysilicon layer while the gate oxide layer, and the first and second spacer are silicon oxide layers.

48. (Original) The ESD protection device as claimed in claim 41 further comprising a fourth doping region enclosing the isolation region.

49. (Original) The ESD protection device as claimed in claim 48, wherein the substrate is a P substrate, the first, second and third doping regions are N doping regions, and the fourth doping region is a P doping region.

50. (Previously Presented) An ESD protection device comprising:

a substrate;

an isolation region on the substrate, enclosing an active region;

a first gate having two ends overlapping the isolation region to stretch over the active region, and coupled to a first node; and

first and second doping regions at the first and second sides of the first gate, and coupled to a second and the first node respectively;

wherein the isolation region protruding into the second doping region near the first end of the first gate.

51. (Original) The ESD protection device as claimed in claim 50, wherein the isolation region is a shallow trench isolation.

52. (Original) The ESD protection device as claimed in claim 50, wherein the first node is ground while the second node is a pad.

53. (Original) The ESD protection device as claimed in claim 50, wherein the isolation region protruding into the second doping region near the second end of the first gate.

54. (Original) The ESD protection device as claimed in claim 53 further comprising:

a second gate having a first and second end overlapping the isolation region to stretch over the active region, and coupled to the first node, wherein the first doping region is on a first side of the second gate; and

a third doping region on a second side of the second gate, coupled to the second node;

wherein the isolation region protruding into the second doping region near the first and second end of the second gate.

55. (Original) The ESD protection device as claimed in claim 54, wherein each of the first and second gate comprises:

a conducting layer;

a gate oxide layer under the conducting layer; and

a first and second spacer respectively adjacent to two sides of the conducting layer and gate oxide layer.

56. (Original) The ESD protection device as claimed in claim 55, wherein the conducting layer is a polysilicon layer while the gate oxide layer, and the first and second spacer are silicon oxide layers.

57. (Original) The ESD protection device as claimed in claim 50 further comprising a fourth doping region enclosing the isolation region.

58. (Original) The ESD protection device as claimed in claim 57, wherein the substrate is a P substrate, the first, second and third doping regions are N doping regions, and the fourth doping region is a P doping region.

59-103. (Cancelled)

104. (New) An ESD protection device comprising:

a substrate;

an isolation region on the substrate, enclosing an active region;

a first gate having two ends overlapping the isolation region to stretch over the active region; and

two source/drain doping regions at the first and second sides of the first gate, the source/drain doping regions coupled to two nodes respectively, wherein one of the source/drain doping regions has a first discontinuity region without source/drain implantation.